

Version 1.3

PMBus+

Presented by: Mike Jones
Travis Summerlin

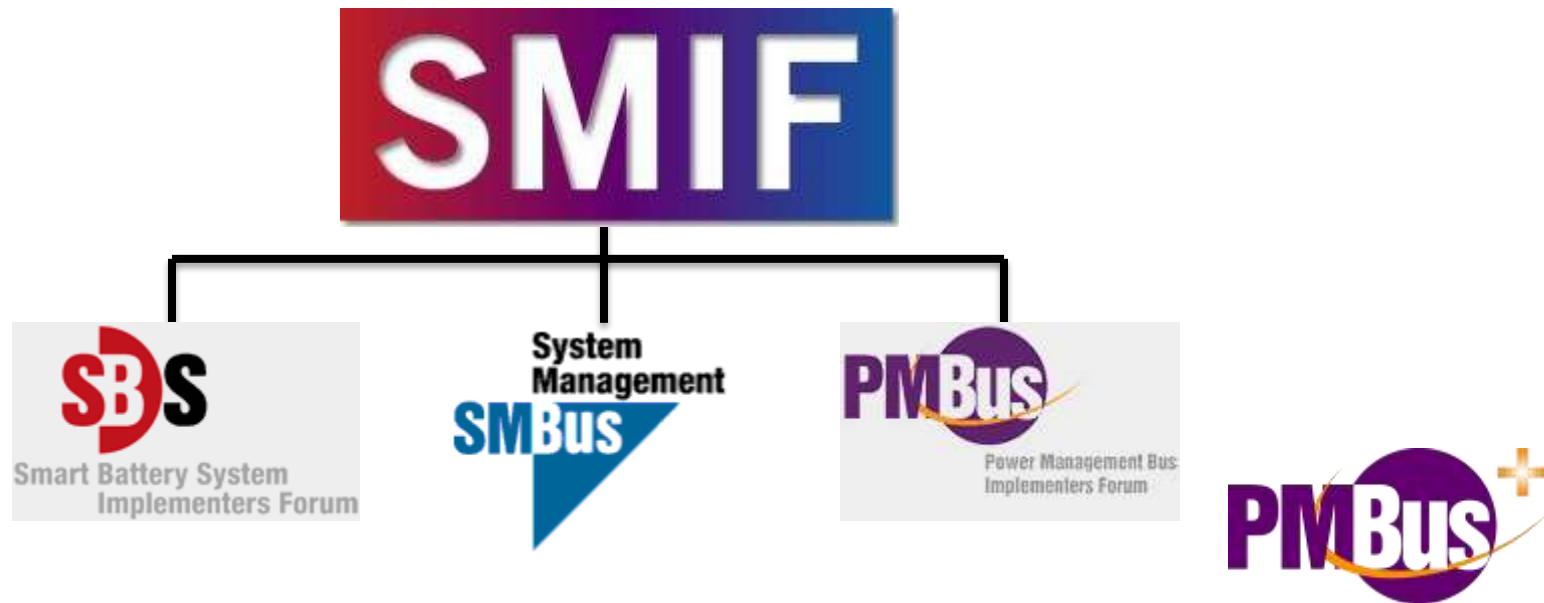
PMBus 1.3 Agenda

- **Introduction**
 - PMBus 1.3 Spec Working Group Charter
- **PMBus 1.3 Overview**
 - Section I & II (Key changes from specification 1.2)
 - Section III (AVS)
- **Timeline**
- **Call to Action**



SMIF/PMBus Organization

- **SMIF** (**S**ystem **M**anagement **I**nterface **F**orum)
 - Supports advancement of a technology base that promotes Power Management and System Technologies implementations
 - Promotes Worldwide inter-operability



PMBus Spec Working Group Charter

IS









- Initiated at the request of customers (Nov 2012)
- Closed group composed mainly of Power Management solution providers that actively participate
- Operating under a charter approved by the PMBus Board of Directors

IS NOT

- Application Profile Committee
- Open Forum initially



Working Group Members

Analog Devices	
Embedded Power Labs	
Emerson Network Power	
Exar	
International Rectifier	
Intersil	
Linear Technology	
Maxim Integrated	
Texas Instruments	



PMBus 1.3 Goals

- **Background**

- PMBus 1.2 is becoming the standard for intelligent power management
- Clear use models and values are emerging

- **Goal**

- Improve upon PMBus 1.2 to address industry use models and values, e.g.
 - Increase Bus throughput as devices increase
 - Address Bus latency for sequencing and fault handling
 - Add Adaptive Voltage Scaling for ASIC, FPGA and processor loads



Target Audience & Disclaimer

- **Target Audience**

- FPGA, ASIC, SoC, Core processors Manufacturers
- OEM Systems Implementers
- Power Management Solution Providers

- **Disclaimer**

- We are presenting the latest draft of the PMBus 1.3 specification. All information is subject to change



PMBus 1.3 Overview

- **PMBus 1.2 vs. PMBus 1.3**
- **Core Enhancements**
 - 1 MHz Bus Speed
 - Floating Point Data Format
 - Relative Voltage Thresholds
 - Global Process Call
 - Adaptive Voltage Scaling



PMBus 1.3 Section I Changes

- **Higher Speed Communications**
 - 1MHz Clock
 - Mandatory Clock Stretching Support
 - Backwards Compatible
- **General Performance Improvement**
 - 2.5X Faster Throughput
 - Same Open Drain Signaling



PMBus 1.3 Section I Changes

- **Floating Point**
 - IEEE 754 Industry Standard
 - Half Precision
 - 16 Bit Number
- **Uniform Number System**
- **Negative Numbers**
- **NaN and +/-Inf**
- **Easy Conversion to C Types**



PMBus 1.3 Section I Changes

- **Global Process Call**
 - Extension of SMBus ARA specification
 - Enables intelligent global queries
- **Applications**
 - Device Discovery
 - Prioritized Fault Management
 - Faster Bulk Reads



PMBus 1.3 Section II Changes

- **Relative Output Voltage Thresholds**
 - Margin Levels
 - Warn Limits
 - Fault Limits
 - Power Good Limits
- **Values Specified as a % of Output Voltage**
- **Changing VOUT_COMMAND Moves All Thresholds**



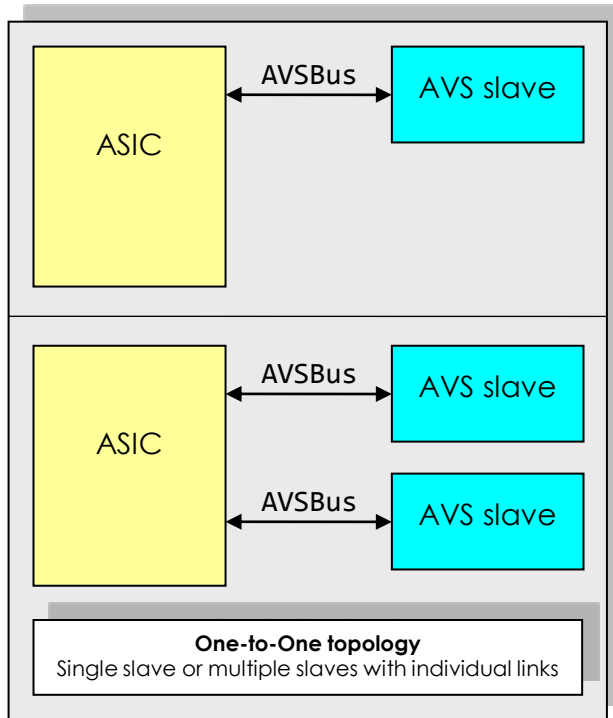
PMBus 1.3 Section III New

- **AVSBus for Adaptive Voltage Scaling**
 - AVSBus is an interface designed to facilitate and expedite communication between an ASIC, FPGA or processor and a POL control device on a system, for the purpose of adaptive voltage scaling
 - When integrated with PMBus, AVSBus is available for allowing independent control and monitoring of multiple rails within one slave



PMBus 1.3 Section III New

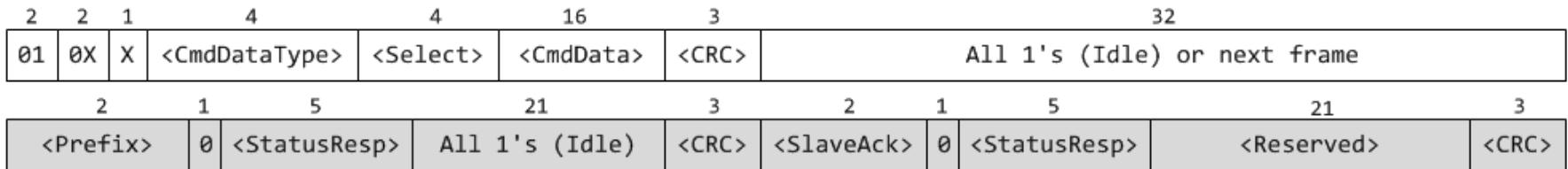
- **AVSBus for Adaptive Voltage Scaling**



- ✓ AVSBus is behaviorally and electrically similar to SPI bus without chip select lines.
- ✓ AVS_MData and AVS_SData are equivalent to MOSI and MISO.
- ✓ AVS_Clock is equivalent to CLK of the SPI bus.
- ✓ 50 MHz max bus speed.

PMBus 1.3 Section III New

- **AVSBus Structure** - All frames are 32 bit
- **Write Frame**



- **Read Frame**



PMBus 1.3 Section III New

- **AVSBus Commands**

- Target Rail Voltage
- Target Rail Vout Transition Rate (Rising and Falling)
- Rail Current (read only)
- Rail Temperature (read only)
- Reset Rail Voltage to Default Value (write only)
- Power Mode (Full Power, Maximum Efficiency)
- AVSBus Status (VGood, OCW, UVW, OTW, OPW)
- AVSBus Version



PMBus 1.3 Section III New

- **AVSBus Commands**

- Feedback from the Slave to the Master

- Asynchronous feedback from the slave by pulling low on the AVS_SData line during idle mode indicating VGood OR an Alert has been generated
- Every frame start by the master generates a status response from the slave
- Every ACK by a slave is followed by a status response from the slave

- Status response

- VGood – VOUT has reached the target voltage
- Alert – One of the bits in the AVSBus Status has been set



PMBus 1.3 Section III New

- **PMBus plus AVSBus integration**
 - AVSBus is an application specific protocol to allow a powered device such as an ASIC, FPGA or Processor to control its own voltage for power savings
 - PMBus is an open standard protocol that defines a means of communicating with power conversion and other devices allowing effective configuration and control as well as telemetry data
 - The combination of these protocols in a slave device is an efficient and effective solution for systems containing loads that need to adapt the operating voltage



Timeline – Release of V1.3

- **Today:** Preliminary information session at DPF to disclose
 - Changes to Section I and II
 - Addition of Section III
- **Through December 1st, 2013:**
 - PMBus Spec Working Group soliciting comments from PMBus Adopters
 - Comments closed December 1st
- **January – March 2014:**
 - Final edits to documents
 - Target Release at APEC 2014 in Fort Worth, TX*

* Target only. Actual release will depend upon the working group working out all technical details.



How to Participate

Step 1 – Be Aware

- Know what's coming
- Understand the impact of AVS to BOTH the power supply/IC community and to the Processor/FPGA/ASIC community

Step 2 – Become a PMBus Adopter (<http://pmbus.org/join.html>)

- Access to documentation at the earliest possible dates

Step 3 – Contact us via [Lodico](#) (PMBus contracted marketing)

- Let us know you're interested
- Set up discussion with Working Group member to discuss impact

Step 4 – Talk to your suppliers & customers

- How do they see PMBus shaping the future



Lodico – Marketing for PMBus 1.3

- **Lodico**

- The PMBus Spec Working Group has contracted Lodico and Company to assist in the promotion and adoption of the revised PMBus 1.3 specification
- Lodico will specifically reach out to new potential PMBus members such as processor, ASIC and FPGA companies to spread awareness of PMBus 1.3 addition of Adaptive Voltage Scaling (AVS)
- Lodico will continue to communicate events and issues regarding the release of PMBus 1.3 to the market until the specification is released

phone: 978.369.6556 or
email: isabran@lodicoandco.com



Call to Action

- **If you are power supply/power IC supplier**
 - Learn how the pending PMBus 1.3 might impact your roadmap
 - Understand that a wide adoption of PMBus 1.3 AVS is able to replace a significant amount of proprietary AVS techniques used in the market today
 - After PMBus 1.3 is ratified, work with your customers on an adoption cycle
- **If you are a processor/ASIC/FPGA/digital supplier**
 - Be aware of what PMBus 1.3 can do to increase system level performance
 - Work with your power IC suppliers to drive an intercept point between your technology and the PMBus market's technology

